WHAT IS CLAIMED IS:

1	1. An ihtegrated circuit, comprising:
2	a transistor level comprising one or more semiconductor devices disposed over a
	substrate and an overlying transistor isolation layer having one or more contact vias
3	extending therethrough;
4	•
5	a ferroelectric device level comprising one or more ferroelectric capacitors
6	disposed over the transistor isolation layer and an overlying ferroelectric isolation layer
7	having one or more vias extending therethrough and laterally sized larger than
8	corresponding contact vias aligned therewith;
9	a first metal level disposed over the ferroelectric device level;
10	an inter-level dielectric level disposed over the first metal level; and
11	a second metal level disposed over the inter-level dielectric level.
1	2. The subject matter of claim 1, wherein the contact vias are filled with
2	tungsten contact plugs.
1	3. The subject matter of claim 2, wherein the ferroelectric capacitors are
2	formed over respective tungsten contact plugs.
1	4. An integrated circuit, comprising:
2	a transistor level comprising one or more semiconductor devices disposed over a
3	substrate and an overlying transistor isolation layer having one or more contact vias
4	extending therethrough;
5	an integrated first metal and ferroelectric device level comprising one or more
6	first metal contacts and one or more ferroelectric capacitors disposed over the transistor
7	isolation layer and a ferroelectric isolation layer having one or more vias extending
8	therethrough;
9	an inter-level dielectric level disposed over the integrated first metal and
10	ferroelectric device level; and
11	a second metal level disposed over the inter-level dielectric level.
1	5. The subject matter of claim 4, wherein the contact vias are filled with
2	tungsten contact plugs.

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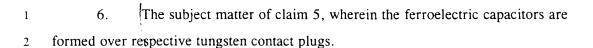
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- 7. The subject matter of claim 4, wherein the integrated first metal and ferroelectric device level has a thickness corresponding substantially to the ferroelectric capacitor heights.
- 8. The subject matter of claim 4, wherein the integrated first metal and 1 ferroelectric device level is substantially non-planar with a reduced thickness in non-2 capacitor regions. 3
 - 9. An integrated circuit, comprising:
 - a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;
 - a first metal level disposed over the transistor isolation layer;
 - a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the first metal level and an overlying ferroelectric isolation layer having one or more vias extending therethrough;
 - an inter-level dielectric level disposed over the ferroelectric device level; and a second metal level disposed over the inter-level dielectric level.
- The subject matter of claim 9, wherein the contact vias are filled with 10. tungsten contact plugs. 2
 - 11. The subject matter of claim 10, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.
 - 12. An integrated circuit, comprising:
- 2 a transistor level comprising one or more semiconductor devices disposed over a 3 substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough; 4
- 5 a first metal level disposed over the transistor isolation layer;
- an inter-level dielectric level disposed over the first metal level; 6

forming a ferroelectric device level comprising one or more ferroelectric

capacitors disposed over the transistor isolation layer and an overlying ferroelectric

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- 1 23. The subject matter of claim 22, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.
- 1 24. The subject matter of claim 21, wherein the integrated first metal and 2 ferroelectric device level has a thickness corresponding substantially to the ferroelectric 3 capacitor heights.

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tungsten contact plugs.

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1	25. The subject matter of claim 21, wherein the integrated first metal and
2	ferroelectric device level is substantially non-planar with a reduced thickness in non-
3	capacitor regions.
1	26. A method of forming an integrated circuit, comprising:
2	forming a transistor level comprising one or more semiconductor devices
3	disposed over a substrate and an overlying transistor isolation layer having one or more
4	contact vias extending therethrough;
5	forming a first metal level over the transistor isolation layer;
6	forming a ferroelectric device level comprising one or more ferroelectric
7	capacitors disposed over the first metal level and an overlying ferroelectric isolation
8	layer having one or more vias extending therethrough;
9	forming an inter-level dielectric level over the ferroelectric device level; and
10	forming a second metal level over the inter-level dielectric level.
1	27. The subject matter of claim 26, wherein the contact vias are filled with
2	tungsten contact plugs.
1	28. The subject matter of claim 27, wherein the ferroelectric capacitors are
2	formed over respective tungsten contact plugs.
1	29. A method of forming an integrated circuit, comprising:
2	forming a transistor level comprising one or more semiconductor devices
3	disposed over a substrate and an overlying transistor isolation layer having one or more
4	contact vias extending therethrough;
5	forming a first metal level over the transistor isolation layer;
6	forming an inter-level dielectric level over the first metal level;
7	forming a ferroelectric device level comprising one or more ferroelectric
8	capacitors disposed over the inter-level dielectric level and an overlying ferroelectric
9	isolation layer having one or more vias extending therethrough; and
10	forming a second metal level over the ferroelectric isolation layer.

The subject matter of claim 29, wherein the contact vias are filled with

- 1 31. The subject matter of claim 30, wherein the ferroelectric capacitors are 1 formed over respective tungsten contact plugs. 2 1 32. A method of forming an integrated circuit, comprising: forming a transistor level comprising one or more semiconductor devices 2 disposed over a substrate and an overlying transistor isolation layer having one or more 3 contact vias extending therethrough; 4 forming a ferroelectric device level comprising one or more ferroelectric 5 6 capacitors disposed over the transistor isolation layer and an overlying ferroelectric isolation layer having one or more vias extending through the ferroelectric isolation 7 8 layer and the transistor isolation layer; 9 forming a first metal level over the ferroelectric device level; forming an inter-level dielectric level over the first metal level; and 10 forming a second metal level over the inter-level dielectric level. 11 < N
- 1 33. The subject matter of claim 32, wherein the contact vias are filled with 2 tungsten contact plugs.
 - 34. The subject matter of claim 33, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

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